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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Michael Violette

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EXAMINER

FARAHANI, DANA

ART UNIT

PAPER NUMBER

2891

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/921,948

Applicant(s)

VIOLETTE, MICHAEL

Examiner

Dana Farahani

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 10-38 and 40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 10-38 and 40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 38 and 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the phrase “a base having a first portion and a second portion having a lateral extent in contact with the emitter to define an emitter-base surface” is indefinite, since it is not clear as to which portion of the base the emitter makes contact to.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 10 and 25-29 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA).

Regarding claims 10 and 25, AAPA discloses in figure 1, a transistor, comprising:

an emitter having an emitter surface area;

a base having a base surface area forming an intrinsic base and an extrinsic base (shown as P+ base), wherein the emitter surface area is in contact with the intrinsic base;

a collector (N well) in contact with the base; and

an implant region (shown as LOCAL IMPLANT) intermediate the base and the collector, the implant region having an implant surface area in contact with the intrinsic base and not in contact with the extrinsic base, the implant surface area being greater than the emitter surface area and less than the intrinsic base surface area, as can be seen in the figure.

Regarding claim 26, the collector has a collector surface area, and the implant region surface area is less than the collector surface area, as can be seen in the figure.

Regarding claim 27, the base surface area is less than the collector surface area.

Regarding claim 28, the base surface area and the implant region surface area where both contact the collector have a combined area greater than the emitter surface area, as can be seen in the figure.

Regarding claim 29, the base directly contacts both the collector and the implant region, as can be seen in the figure.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 17-24 and 30-32, and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grubisich (US Patent 5,581,115).

Regarding claims 17 and 23, Grubisich discloses in figure 2, a transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity

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which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region 42 having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

a base region 52 having an impurity therein which promotes the first majority carrier, the base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region 50 on the base region, the emitter region having a surface area smaller than a surface area of the base region;

a first implant region 58 interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective surface area greater than the surface area of the emitter region contiguous to the base region and less than the area of the base region contiguous to the collector region.

Grubisich does not disclose in this figure, a second implant region formed in the collector region.

Grubisich discloses in figure 5a, an implant region 90 in the BJT device shown in that figure. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a second implant area in the collector region in order to make a collector contact.

Regarding claim 18, the second implant region would be formed at about the same level from the surface of the substrate as the first implant.

Regarding claims 19, 20, and 34-37, Grubisich discloses the limitations in these claims, as discussed above with respect to claim 17. Also, note that the implant region 90 is formed in the plug region, that is the region that directly surrounds region 90. Also, a sub-region of region 90 at the same depth of the implant region 58 forms the second implant in region 90.

Regarding claims 21, 22, and 31, see Grubisich, column 12, lines 31-34, wherein it is stated that boron and phosphorus are used to make the p and n regions of the device, respectively (note that Grubisich discloses at column 16, lines 42-44 that a pnp transistor can be used as well).

Regarding claim 24, the second implant (the middle portion of plug 90) in figure 5a has a surface area greater than the surface area of the opening at the top of it.

Regarding claim 30, Grubisich discloses in figure 2, a transistor device formed in a semiconductor substrate comprising:

- an n well collector region having an impurity of a first conductivity type, the collector region extending downwardly from a surface of the substrate, the substrate being generally doped with an impurity of a second conductivity type;

- a base region 52 and 54 having an impurity of the second conductivity type doped at a generally constant doping level across a surface thereof, the base region extending downwardly from the surface of the substrate into contact with a portion of the collector region;

- an emitter 50 having an impurity of the first conductivity type on top of the base region and having a surface area smaller than a surface area of the base region; and

- an area of the collector region vertically adjacent the base region having an increased

collector doping of the first conductivity type, the area of the collector region having an effective surface area in contact with the base region that is substantially greater than the surface area of the emitter and substantially smaller than the surface area of the base region, as can be seen in the figure.

Regarding claim 32, the effective surface area of the collector region is less than a non-increased doped area of the portion of the collector region (region 42) in contact with the base region, as can be seen in the figure.

7. Claims 13-16 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Grubisich.

Regarding claims 13, 16 and 33, AAPA discloses in figure 1, a transistor formed in a substrate, the transistor comprising:

a collector region (shown as N WELL) having a first impurity means for promoting one of either holes or electrons as a majority carrier, the collector region extending downward from the surface of the substrate;

a base region (BASE) having a second impurity means for promoting the other type of carrier with a first portion, intrinsic, of the base, having a first impurity level and a second (extrinsic) portion (shown as P+), of the base having a second higher impurity level, the base region having a surface area and extending downward from the surface of the substrate into contact with a portion of the collector region;

an emitter region (N+ EMITTER) on top of the first portion of the base region and having a surface area smaller than the surface area of the first portion of the base region; and

an implant area (LOCAL IMPLANT) of the collector region vertically adjacent to the first portion of the base region having an increased collector doping of an implanted impurity, the implant area having an effective surface area that is in contact with the base region, greater than the surface area of the emitter region and less than the surface area of the first portion of the base region, as can be seen in the figure.

AAPA does not disclose a substrate with an impurity of a conductivity type other than that of the collector.

Grubisich discloses in figure 2, a substrate with an impurity of an opposite type to the collector, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the substrate of the AAPA as an opposite conductivity type substrate with respect to the collector for operational purposes of the transistor.

Regarding claims 14 and 15, Grubisich discloses the transistor can be an NPN as well as a PNP transistor (see above).

8. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as applied to claim 10 above, and further in view of Grubisich.

AAPA discloses the limitations in the claims, as discussed above, except for disclosing that boron and phosphorus are used to dope the collector region.

Grubisich discloses that these materials are used to dope the regions of the transistor therein, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use boron and phosphorus to dope the collector region of the AAPA device, since it is well known to use these material as doping agent of semiconductor devices.



***Product-by-Process Limitations***

In claims 36 and 37, the implant regions “being simultaneously formed by an angled implant”, or “by the same source” are considered methods of forming those regions and not limitations of the final product. Therefore, such limitations are given no patentable weight.

The Office reminds Applicant that “product by process” limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

***Allowable Subject Matter***

9. Claims 38 and 40 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

***Response to Arguments***

10. Applicant's arguments with respect to the previously rejected claims have been considered but are moot in view of the new grounds of rejection.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

  
HOAI PHAM  
PRIMARY EXAMINER